LESSON PLAN:–2023-2024

DISCIPLINE: ETC	**SEMESTER: 5TH**	**NAME OF THE TEACHING FACULTY:- ANURAG SETHY**
SUBJECT:- VLSI LAB	**NO.OF periods / PER WEEK :1 1period:3hrs**	**SEMESTER FROM DATE:- 01/07/2024 TO DATE: 16/12/2024 NO.OF WEEKS:-15**
WEEK	CLASS DAY	PRACTICAL TOPICS
1ST	1ST	Introduction to VLSI design using VHDL code importants of VLSI design & Advantages.
2ND	1ST	Learn about VLSI design using VHDL layout of various Logic gates.
3RD	1ST	Student should do hands on practice about VLSI design using VHDL layout of various Logic gates & note the observations.
4TH	1ST	Learn about VLSI design using VHDL & implementation of Half Adder & Full Adder.
5TH	1ST	Student should perform & design VLSI using VHDL & implement of Half Adder& note the observations.
6TH	1ST	Student should perform & design VLSI using VHDL & implement of Full Adder & note the observations
7TH	1ST	Learn how to develop a VHDL test bench code & implement of MUX & DEMUX
8TH	1ST	Student should perform & design VLSI using VHDL & implement for MUX & note the observations
9TH	1ST	Student should perform & design VLSI using VHDL & implement for MUX (8:1) & note the observations
10TH	1ST	Student should perform & design VLSI using VHDL & implement for DEMUX (1:8) & note the observations
11TH	1ST	Learn how to develop a VHDL test bench code & implement of ENCODER with or without priority.
12TH	1ST	Student should perform & design VHDL test bench code & implement of ENCODER with priority
13TH	1ST	Student should perform & design VHDL test bench code & implement of ENCODER without priority
14TH	1ST	**Small project implementation by VHDL CODE**
15TH	1ST	**Practical Assesment**