U. G. M. I. T, RAYAGADA DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGG ACADEMIC LESSON PLAN FOR WINTER SEMESTER-2023 NAME OF THE FACULTY | Smita Patnaik **DEPT ETC SEMESTER** 3rd **SUBJECT Digital Electronics** NO. OF PERIODS PER WEEK 4 **TOTAL PERIODS** 60 80 20 **END SEMESTER EXAM CLASS TEST** TOTAL MARKS 100 **TOPIC TO BE COVERED WEEK UNIT/ CHAPTER PERIOD** Digital electronics fundamentals 1st 2nd Number system binary, octal, decimal and hexadecimal 1st Convertiion from one system to other 3rd 4th Arithmetic operation addition, subtraction, multiplication etc 1st 1s and 2s complement of binary numbers BASICS OF DIGITAL Digital codes and its application 2nd 2nd **ELECTRICS** 3rd Logic gates 4th Universal gates and its realization 1st **Demorgans theorm** SOP and POS form 2nd 3rd 3rd 3 variable karnaugh map 4th 4 variable karnaugh map 1st Half adder and full adder Half subtractor 2nd 4th 3rd Multiplexer 4*1 Multiplexer 4*1 4th Seven segment decoder 1st **COMBINATIONAL LOGIC** Concept of full subtractoe 2nd 5th **CIRCUITS** concept of full subtractor 3rd 4th Concept of encoder 1st Digital comparator 2nd Application of seven segment decodee 6th 3rd Application of seven segment decoder 4th Serial to parallel converter Principles of flip flop operation 1st 2nd SR flip flop using NAND latch 7th SR flip flop using NOR latch 3rd 4th Concept of SR flipflop 1st Concept of JKflip flop Concept of Masterslave flip flop 2nd **SEQUENTIAL LOGIC** 8th **CIRCUITS** 3rd Logic circuit and truth table of T flip flop Logic circuit and truth table of D flip flop 4th Application of master slave flip flop 1st Concept of racing 2nd 9th 3rd How racing can be avoided

How racing can be avoided

Shift registers

4th 1st

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10th	2nd	REGISTERS, MEMORIES & PLD	Universal shift registers
	3rd		Application of shift registers
	4th		Type of counters
11th	1st		Binary counter and asynchronous ripple counter
	2nd		Ring counter
	3rd		Concept of RAM, ROM, SRAM etc
	4th		Concept of PLD and application
12th	1st	A/D & D/A CONVERTERS	Necessity of A/D and D/ A converter
	2nd		D/A converter using weighted register
	3rd		D/A convertion using R 2R ladder
	4th		A/ D convertion using counter method
13th	1st		A/D convertion using counter method
	2nd		Successive approximate method
	3rd		Successive approximate method
	4th		Various logic families
14th	1st		IC fabrication process
	2nd		Characteristics of digital ics
	3rd		propagation delay, fan in, fan out
	4th	LOGIC FAMILIES	Power dissipation and noise marginand power supply
15th	1st		Speed with reference to logic families
	2nd		Features of TTL
	3rd		Features of CMOS(NAND and NOR)
	4th		Features of CMOS(NAND and NOR)