LESSON PLAN – 2022 -2023

DISCIPLINE: ETC	**SEMESTER : 5th**	**NAME OF THE TEACHING FACULTY: ANURAG SETHY**
SUBJECT: VLSI AND EMBEDDED SYSTEM	**NO.OF DAYS/PER WEEK CLASS ALLOTTED : 4**	**SEMESTER FROM DATE: 15/09/2022 TO DATE: 22/12/2022 NO.OF WEEKS:15**
WEEK	**CLASS DAY**	**THEORY TOPICS**
1ST	1ST	HISTORICAL PERSPECTIVE- INTRODUCTION
	2ND	CMOS DIGITAL CIRCUITS TYPES
	3RD	INTRODUCTION TO MOS TRANSISTOR& BASIC OPERATION OF MOSFET.
	4TH	STRUCTURE AND OPERATION OF MOSFET (N-MOS ENHANCEMENT TYPE)
2ND	1ST	STRUCTURE AND OPERATION OF MOSFET
	2ND	MOSFET V-I CHARACTERISTICS
	3RD	WORKING OF MOSFET CAPACITANCES.
	4TH	MODELLING OF MOS TRANSISTORS INCLUDING BASIC CONCEPT THE SPICE LEVEL-1 MODELS, THE LEVEL-2 AND LEVEL-3 MODEL.
3RD	1ST	FLOW CIRCUIT DESIGN PROCEDURES
	2ND	VLSI DESIGN FLOW & Y CHART
	3RD	DESIGN HIERARCHY, VLSI DESIGN STYLES-FPGA, GATE ARRAY DESIGN
	4TH	STANDARD CELLS BASED, FULL CUSTOM
4TH	1ST	SIMPLIFIED PROCESS SEQUENCE FOR FABRICATION
	2ND	BASIC STEPS IN FABRICATION PROCESSES FLOW
	3RD	FABRICATION PROCESS OF NMOS TRANSISTOR
	4TH	FABRICATION PROCESS OF NMOS TRANSISTOR
5TH	1ST	CMOS N-WELL FABRICATION PROCESS FLOW
	2ND	CMOS N-WELL FABRICATION PROCESS FLOW
	3RD	MOS FABRICATION PROCESS BY N-WELL ON P-SUBSTRATE
	4TH	CMOS FABRICATION PROCESS BY P-WELL ON N-SUBSTRATE
6TH	1ST	LAYOUT DESIGN RULES,
	2ND	STICK DIAGRAMS OF CMOS INVERTER
	3RD	BASIC NMOS INVERTERS,
	4TH	WORKING OF RESISTIVE-LOAD INVERTER
7TH	1ST	INVERTER WITH N-TYPE MOSFET LOAD – ENHANCEMENT LOAD, DEPLETION N-MOS INVERTER
	2ND	ENHANCEMENT LOAD, DEPLETION N-MOS INVERTER
	3RD	CMOS INVERTER – CIRCUIT OPERATION
	4TH	CMOS INVERTER CHARACTERISTICS
8TH	1ST	INTERCONNECT EFFECTS AND DELAY TIME DEFINITIONS
	2ND	CMOS INVENTOR DESIGN
	3RD	DELAY CONSTRAINTS – TWO SAMPLE MASK LAY OUT FOR P-TYPE SUBSTRATE

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	4TH	DEFINE STATIC COMBINATIONAL LOGIC ,WORKING OF STATIC CMOS LOGIC CIRCUITS (TWO-INPUT NAND GATE)
9TH	1ST	DEFINE STATIC COMBINATIONAL LOGIC ,WORKING OF STATIC CMOS LOGIC CIRCUITS (TWO-INPUT NAND GATE)
	2ND	CMOS LOGIC CIRCUITS (NAND2 GATE)
	3RD	CMOS TRANSMISSION GATES(PASS GATE)
	4TH	COMPLEX LOGIC CIRCUITS - BASICS
10TH	1ST	CLASSIFICATION OF LOGIC CIRCUITS BASED ON THEIR TEMPORAL BEHAVIOUR
	2ND	SR FLIP LATCH CIRCUIT,
	3RD	SR FLIP LATCH CIRCUIT,
	4TH	CLOCKED SR LATCH ONLY
11TH	1ST	CMOS D LATCH.
	2ND	BASIC PRINCIPLES OF DYNAMIC PASS TRANSISTOR CIRCUITS
	3RD	BASIC PRINCIPLES OF DYNAMIC PASS TRANSISTOR CIRCUITS
	4TH	DRAM
12TH	1ST	SRAM
	2ND	FLASH MEMORY
	3RD	Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xlinx
	4TH	Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xlinx
13TH	1ST	Design strategies & concept of FPGA with standard cell based design
	2ND	VHDL DESIGN SYNTHESIS USING FPGA
	3RD	RASBERRY PI
	4TH	Embedded Systems Overview,list of embedded systems,characteristics ,example – A Digital Camera
14TH	1ST	Embedded Systems Technologies--Technology – Definition
	2ND	-Technology for Embedded Systems -Processor Technology - IC Technolog
	3RD	Design Technology-Processor Technology
	4TH	General Purpose Processors – Software,
15TH	1ST	Basic Architecture of Single Purpose Processors – Hardware
	2ND	Application – Specific Processors,Microcontrollers,Digital Signal Processors(DSP)
	3RD	IC Technology- Full Custom / VLSI,Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)
	4TH	Basic idea of Arduino